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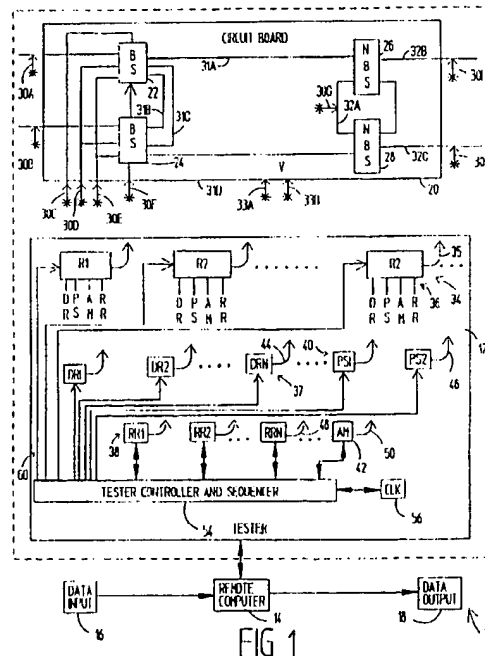
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(54) **Powered testing of mixed conventional/Boundary-Scan Logic.**

(57) The (X,Y) positions of the nodes 31A - 31C, 32A - 32C in a circuit 20 containing boundary scan components 22, 24 and non-boundary-scan components 26, 28 are stored in a computer 14. The computer 14 selects a set 32A - 32C of non-boundary scan nodes within a radius R of a selected boundary-scan node 31A, R being the length of solder bridges in the circuit. A logic 0 voltage is applied to the set 32A - 32C and a boundary-scan test is performed. If the boundary-scan test fails, a fault is declared in the circuit 20 between the set 32A - 32C and the selected boundary-scan node 31A. A logic 1 voltage is applied to one 32A of the nodes in the set 32A - 32C, and the test repeated. If the test returns different results, the fault is declared between that one node 32A and the selected boundary-scan node 31A.



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## EUROPEAN SEARCH REPORT

Application Number  
EP 92 31 0065

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
E	EP-A-0 543 506 (HEWLETT-PACKARD CO.)  * abstract; figure 9 * * page 7, column 11, line 31 - line 45 * * claims 1-3 *  ---	1,2,4, 6-8	G01R31/318 G06F11/26
A	PROCEEDINGS OF THE INTERNATIONAL TEST CONFERENCE, 1990 September 1990 , BALTIMORE, USA pages 572 - 581 G.D. ROBINSON, J.G. DESHAYES 'Interconnect testing of boards with partial boundary scan'  -----	1	
			TECHNICAL FIELDS SEARCHED (Int.Cl.5)
			G06F
The present search report has been drawn up for all claims			
Place of search <b>THE HAGUE</b>		Date of completion of the search <b>12 April 1994</b>	Examiner <b>Sarasua Garcia, L</b>
<b>CATEGORY OF CITED DOCUMENTS</b>			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document	

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